UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SAM B. SANDBOTE

Appeal No. 2006-1450
Application No. 09/933,786

ON BRIEF

Before JERRY SMITH, BARRY, and HOMERE, **Administrative Patent Judges**.

HOMERE, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-33, all of which are pending in this application.

Invention

Appellant's invention relates generally to a shift processing unit (figure 3) for processing an incoming data stream. The shift processing unit includes an N-bit barrel shifter (320) coupled to a shift post processor (340) and a shift carry register (330). The N-bit barrel shifter (320) shifts an incoming operand (315) according to an offset parameter to thereby generate a shifted operand. The shift carry register (330), in turn, transforms the shifted operand into a shift carry operand, which it transfers to the shift post processor (340) to then store both the shifted operand and the shift carry operand in memory. The shift post processor (340) then processes the shifted operand to generate an output based on at least a control signal and a mask field. The shift post processor (340) includes a decoder (710) that it uses to decode the offset parameter into the mask field, wherein the mask field includes a plurality of bits, each mask bit corresponding to a bit position of the shifted operand.

Claim 1 is representative of the claimed invention and is reproduced as follows:

1. An apparatus comprising:

a shift post processor;

a shifter to shift an operand according to an offset parameter, generating a shifted operand; and

a register coupled to the shift post processor capable of transferring a shift carry operand stored in the register to the shift post processor, and coupled to the shifter to store the shifted operand after any transfer of the shift carry operand;

wherein the shift post processor is coupled to the shifter and the register to process the shifted operand to generate an output based on at least a control signal and a mask field, and

wherein the shift post processor comprises a decoder to decode the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand.

References

The Examiner relies on the following references:

Groves	5,222,225	Jun. 22, 1993
Methvin et al.(Methvin)	4,896,133	Jan. 23, 1990
Prioste	4,149,263	Apr. 10, 1979

Rejections At Issue

A. Claims 1, 2, 11, 12, 21 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Groves.[1]

B. Claims 3-10, 13-20 and 23-33 stand rejected under 35 U.S.C. § 103 as being unpatentable over the combination of Groves and Prioste.

Rather than reiterating the arguments of Appellant and the Examiner, the opinion refers to respective details in the Appeal Brief[2] and the Examiner's Answer.[3] Only those arguments actually made by Appellant have been considered in this decision. Arguments that Appellant could have made but chose not to make in the Brief have not been taken into consideration. See 37 CFR 41.37(c)(1) (vii) (eff. Sept. 13, 2004).

OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the Examiner's rejection, the arguments in support of the rejection and the

1 This rejection was also reinforced by Methvin et al as evidence of what's well known in the art.
2 Appellants filed an Appeal Brief on July 18, 2005.
3 The Examiner mailed an Examiner's Answer on September 19, 2005.

evidence of obviousness relied upon by the Examiner as support for the rejections. We have likewise reviewed and taken into consideration Appellant's arguments set forth in the Appeal Brief along with the Examiner's rationale in support of the rejection and arguments in the rebuttal set forth in the Examiner's Answer.

After full consideration of the record before us, we agree with the Examiner that claims 1, 2, 11, 12, 21 and 22 are properly rejected under 35 USC 103 as being obvious over Groves. We further agree with the Examiner that dependent claims 3-10, 13-20 and 23-33 are properly rejected over the combination of Groves and Prioste. Accordingly, we affirm the Examiner's rejection of claims 1-33 for the reasons set forth **infra**.

I. Under 35 USC 103, is the Rejection of Claims 1, 2, 11, 12, 21 and 22 as Being Unpatentable over Groves Proper?

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of establishing a **prima facie** case of obviousness. **In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). **See also In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). The Examiner can satisfy this burden by showing that some objective teaching in

the prior art or knowledge generally available to one of ordinary skill in the art suggests the claimed subject matter. **In re Fine**, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Only if this initial burden is met does the burden of coming forward with evidence or argument shift to the Appellants. **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. **See also Piasecki**, 745 F.2d at 1472, 223 USPQ at 788.

An obviousness analysis commences with a review and consideration of all the pertinent evidence and arguments. ``In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument.'' **Oetiker**, 977 F.2d at 1445, 24 USPQ2d at 1444. ``[T]he Board must not only assure that the requisite findings are made, based on evidence of record, but must also explain the reasoning by which the findings are deemed to support the agency's conclusion.'' **In re Lee**, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

With respect to claims 1, 2, 11, 12, 21 and 22, Appellant argues at page 3 of the Appeal Brief that Groves does not teach that each of the masked bits corresponds to a bit position of the

shifted operand. In particular, at page 3 of the Appeal Brief, Appellant states the following:

> "Among other deficiencies, the reference does not teach or suggest the limitations in claims 1, 11 and 21 that each of the masked bits corresponds to a bit position of the shifted operand. This mask allows for shifting by any number of bits, from 1 to the length of the word. Groves is directed to the manipulation of text strings where each character occupies an entire byte (col. 2, lines 44-47). Groves teaches shifting only by entire bytes. There is no teaching or suggestion that shifting be done at the bit level. In fact, Groves teaches against this. If text strings were shifted by numbers of bits other than entire bytes, then the bits making up each character would be spread across two bytes. When such shifted text is read byte-by-byte, the correct characters would not be present."

In order for us to decide the question of obviousness, "[t]he first inquiry must be into exactly what the claims define." **In re Wilder**, 429 F.2d 447, 450, 166 USPQ 545, 548 (CCPA 1970). "Analysis begins with a key legal question-- what is the invention claimed ?"...Claim interpretation...will normally control the remainder of the decisional process." **Panduit Corp. v. Dennison Mfg.**, 810 F.2d 1561, 1567-68, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), **Cert denied**, 481 U.S. 1052 (1987).

We note that independent claim 1 reads in part as follows:

> "The shift post processor comprises a decoder to decode the offset parameter into the mask field, the mask field having a plurality of bits, each of the mask bits corresponding to a bit position of the shifted operand."

At page 11, paragraph 0054, Appellant's specification states:

> The decoder 710 receives the OFFSET parameter and generates a shift field mask MASK [1 . . . N]. The shift field mask has N bits, mask(1) to mask (N), corresponding to N-bit word of the shifted operand. The shift mask field defines the bit positions that are affected by the post processing operations. In one embodiment, a logical one in the mask(k) indicates that the bit at the k-th position is affected by the post processing operation, and a logical zero allows the bit at the k-th position to pass through unmodified. The decoder essentially converts the OFFSET value into a bit pattern having a group of consecutive mask bits that corresponds to the portion of the operand to be operated upon.

Thus, the claim does require that each of the masked bits corresponds to a bit position of the shifted operand.

Now, the question before us is what Groves would have taught to one of ordinary skill in the art? To answer this question, we find the following facts:

1. Groves states, at column 1 lines 22-28, that:

> In modern data processing systems, this storage unit of data is termed a word and consist of 16 binary digits or bits. Words may also consist of 32, 48 or 64 bits

depending on the characteristic of the specific data processing system. It is also desirable to break up words into smaller units such as bytes (8 bits), or nibbles (4 bits).

2. Groves states, at column 4, lines 63-68, that:

The Load Byte Merge Mask controls the Byte Merge 30. A '1' indicates that this byte from memory 20 should replace this byte from Register 26. A '0' indicates that the byte from Register 26 should be used as is. The control logic 14 generates the Load Byte Merge Mask as shown in Table 1.

3. Groves states, at column 5, lines 1-7, that:

The Last Access Mask bits are used to control the Byte Merge 30 for the last access. A '1' indicates that this byte should be passed through as controlled by the Load Byte Merge Mask. A '0' indicates that a value of binary '00000000' should be passed for this byte. The control logic 14 generates the Last Access Mask bits as shown in Table 2.

4. Groves states, at column 5, lines 41-47, that:

The Store Byte Merge Mask controls the Byte Merge 60. A '1' indicates that this byte from register 56 should replace this byte from the General Purpose Register File 44. A '0' indicates that the byte from the General Purpose Register File 33 should be used as is. The control logic 14 generates the Store Byte Merge Mask as shown in Table 3.

5. Methvin et al. state, at column 11, lines 28-32, that:

After a portion of a data string is loaded into flip-flops 196 of the shift registers 186, 188, the portion Periodically shifted either one bit or eight bits at a time, depending on whether the processor is performing a bit-by-bit comparison or a byte-by-byte comparison.

6. Methvin et al. state, at column 16, lines 51-52, that:

> The bit mode of operation of the processor is generally similar to its byte mode of operation.

With the above discussion in mind, we find that the Groves reference teaches the claimed invention. First, Groves is relied upon, inter alia, for its teaching of a byte merge logic (30) coupled to a byte rotator (22) and a register (26), wherein the byte merge logic (30) generates outputs (42) based in-part on control signals including a mask field (e.g. Load Byte Merge Mask) received from the control logic (14) to help identify which data byte from memory that should be shifted. We agree with the Examiner that one of ordinary skill in the art would have readily been apprised of the fact that a byte is generally known as 8 bits. Therefore, the ordinary skilled artisan would have recognized that shifting an entire byte is equivalent to shifting 8 bits (i.e. a plurality of bits). Furthermore, as indicated in the Methvin reference, the ordinary skilled artisan would have also known that a bit mode of operation of the processor is similar to its byte mode of operation. Thus, the ordinary skilled artisan would have found it obvious to substitute the well-known

bit operation for the byte operation disclosed in Groves to thereby yield the claimed limitation, whereby each of the masked bits corresponds to a bit position of the shifted operand.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the invention as set forth in claims 1, 2, 11, 12, 21 and 22. Accordingly, we will sustain the Examiner's rejection of claims 1, 2, 11, 12, 21 and 22 over the Groves reference.

II. Under 35 USC 103, is the Rejection of Claims 3-10, 13-20 and 23-33 as Being Unpatentable over Groves Proper?

With respect to dependent claims 3-10, 13-20 and 23-33, Appellant argues at page 5 of the Appeal Brief that Groves does not teach that each of the masked bits corresponds to a bit position of the shifted operand. Appellant also argues that Prioste does not cure these deficiencies. We addressed this argument in the discussion of claim 1 above, and we found that the combination of Groves' teaching with knowledge of the ordinary skilled artisan would have rendered the claimed invention obvious. Appellant also argues that there is no

motivation to combine the references, and that there is no showing that it would provide a reasonable expectation of success. We note that Prioste was relied upon for its teaching of bit shifting with sign and zero extension. We also find that Prioste provides adequate motivation for combining its teachings with that of Groves. Particularly, at column 1, lines 42-44, Prioste indicates that its suggested approach increases the processing time of the data and reduce the cost of circuitry used for shifting. Therefore, the combination of Groves and Prioste was proper and would thus provide a reasonable expectation of success.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the invention as set forth in dependent claims 3-10, 13-20 and 23-33. Accordingly, we will sustain the Examiner's rejection of claims 3-10, 13-20 and 23-33 over the combination of Groves and Prioste.

CONCLUSION

In view of the foregoing discussion, we have sustained the Examiner's decision rejecting claims 1-33 under 35 U.S.C. § 103. Therefore, we affirm.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

JERRY SMITH)
Administrative Patent Judge)
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) BOARD OF PATENT
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